WHAT IS CLAIMED IS:

1. A process for fabricating a vertical transistor comprising:

forming a first device region selected from the group consisting of a source region and a drain region of a semiconductor device in a semiconductor substrate;

forming a multilayer stack comprising at least three layers of material over the first device region in the semiconductor substrate wherein the second layer is interposed between the first and the third layers and wherein the first layer is proximate the first device region;

forming a window in the at least three layers of material, wherein the window terminates at the first device region formed in the semiconductor substrate;

forming semiconductor material, of a first conductivity type, within the window, thereby forming a semiconductor plug in the at least three layers of material, wherein the semiconductor plug has a first end, and a second end, and wherein the first end is in contact with the first device region;

forming a second device region selected from the group consisting of a source region and a drain region at the second end of the silicon plug, wherein one of the first and second device regions is a source region and the other is a drain region;

removing the second layer, thereby exposing a portion of the semiconductor plug; and

forming a gate in contact with the semiconductor plug, wherein the gate is of a second conductivity type.

2. The process of claim 1 wherein the second layer is removed by etching in an etchant, wherein the first layer has a first etch rate, the second layer has a second etch rate, and the third layer has a third etch rate, and wherein the second etch rate is at least ten times faster than the first etch rate and the third etch rate in the etchant.

3. The process of claim 2 wherein the first layer and the third layer are made of an electrically insulating material.

4. The process of claim 3 wherein the electrically insulating material is selected from silicon nitride, silicon dioxide, and doped silicon dioxide.

5. The process of claim 3 wherein the electrically insulating material is doped silicon dioxide that serves as a dopant source for a source extension and a drain

extension, and wherein the process further comprises the step of doping the semiconductor plug with dopant from the first layer and the third layer to form the source and drain extensions in the semiconductor plug.

6. The process of claim 5 wherein the type of dopant in the doped silicon dioxide is selected from the group consisting of n-type and p-type, and wherein the dopant is opposite the dopant type in the semiconductor plug.

7. The process of claim 1 wherein the semiconductor plug comprises a doped semiconductor plug, and wherein the dopant is selected from the group consisting of n-type dopants and p-type dopants.

8. The process of claim 7 wherein the semiconductor material comprises a crystalline semiconductor material and is selected from the group consisting of silicon, silicon germanium, and silicon-germanium-carbon.

9. The process of claim 1 further comprising the step of forming an insulating layer over the first layer of material, or over the second layer of material, or over both the first and the second layers of material.

10. The process of claim 9 wherein the layer of insulating material comprises an etch stop layer.

11. The process of claim 9 wherein the layer of insulating material comprises an offset spacer.

12. The process of claim 1 further comprising the step of chemical mechanical polishing the surface of the substrate after forming the semiconductor plug, wherein the chemical mechanical polishing planarizes the semiconductor plug with the third layer of the multilayer stack.

13. The process of claim 12 wherein the top layer of material in the multilayer stack comprises a stop for chemical mechanical polishing.

14. The process of claim 12 wherein the top layer of material in the multilayer stack comprises a silicon nitride layer.

15. The process of claim 1 further comprising the step of forming a diffusion barrier layer over the first device region before the at least three layers of material are formed thereover.

16. The process of claim 1 further comprising the steps of forming a layer of oxide on the exposed portion of the semiconductor plug, removing the layer of oxide, and forming the gate on the exposed portion of the semiconductor plug, wherein the gate is of opposite conductivity-type to the semiconductor plug.

17. The process of claim 1 further comprising the step of forming a region of a second conductivity type surrounding the first conductivity type region of the semiconductor plug.

18. The process of claim 1 wherein the gate is of a second conductivity type, and further comprising the step of doping a region of the semiconductor plug from the gate to form a pn junction in the semiconductor plug.

19. The process of claim 1 wherein the substrate is selected from the group consisting of silicon substrates and silicon-on-insulator substrates.

20. The process of claim 1 wherein the gate material is selected from the group consisting of doped polycrystalline silicon, doped amorphous silicon, doped silicon germanium, silicon-germanium-carbon, metal, and metal compounds.

21. The process of claim 20 wherein the gate material is formed on the substrate by chemical vapor deposition, electroplating, or a combination thereof.

22. The process of claim 20 wherein the metals and metal compounds are selected from the group consisting of titanium, titanium nitride, tungsten, tungsten silicide, tantalum, tantalum nitride, molybdenum, aluminum and copper.

23. A process for fabricating an integrated circuit structure comprising:

forming a first device region selected from the group consisting of a source region and a drain region of a semiconductor device in a semiconductor substrate;

forming a multilayer stack comprising at least three layers of material over the first device region in the semiconductor substrate, wherein the second layer is interposed between the first and the third layers, and wherein the first layer is adjacent the first device region;

forming a first and a second window in the at least three layers of material, wherein said first and second windows terminate at the first device region formed in the semiconductor substrate;

forming a semiconductor material within the first and the second windows, thereby forming a first and a second semiconductor plug in the at least three layers of material, wherein each of the first and the second semiconductor plugs has a first end and a second end, and wherein the first end of each semiconductor plug is in contact with the first device region, and wherein the first semiconductor plug is of a first conductivity type;

forming a second device region selected from the group consisting of a source region and a drain region at the second end of the first semiconductor plug, wherein one of the first and second device regions is a source region and the other is a drain region;

forming a third device region selected from the group consisting of a source region and a drain region at the second end of the second semiconductor plug, wherein one of the first and the third device regions is a source region and the other is a drain region;

removing the second layer, thereby exposing a portion of the first and the second semiconductor plugs;

forming a layer of dielectric material on the exposed portion of the first semiconductor plug;

forming a region of a second conductivity type surrounding the first conductivity type region of the second semiconductor plug; and

forming a gate having a first region in contact with the layer of dielectric material and having a second region in contact with the second conductivity type region of the second semiconductor plug.

24. The process of claim 23 wherein the gate is of a second conductivity type, and further comprising the step of doping a region of the second semiconductor plug from the gate to form a pn junction in the semiconductor plug.

25. The process of claim 23 wherein the second layer is removed by etching in an etchant, wherein the first layer has a first etch rate, the second layer has a second etch rate, and the third layer has a third etch rate, and wherein the second etch rate is at least ten times faster than the first etch rate and the third etch rate in the etchant.

26. The process of claim 24 wherein the etchant is selected from the group consisting of isotropic wet etchants and isotropic dry etchants.

27. The process of claim 23 wherein the first layer and the third layer are formed of electrically insulating material.

28. The process of claim 27 wherein the electrically insulating material is selected from silicon nitride, silicon dioxide, doped silicon dioxide, and doped silicon oxide.

29. The process of claim 27 wherein the electrically insulating material comprises doped silicon dioxide that is a dopant source for a source extension and a drain extension, and wherein the process further comprises the step of doping the semiconductor plug with dopant from the first layer and the third layer to form source and drain extensions in the semiconductor plug

30. The process of claim 29 wherein the type of dopant in the doped silicon dioxide is selected from the group consisting of n-type and p-type, and wherein the dopant type is opposite the dopant type in the first and the second semiconductor plugs.

31. The process of claim 23 wherein the first and the second semiconductor plugs comprise doped semiconductor plugs, and wherein the dopant is selected from the group consisting of n-type dopants and p-type dopants.

32. The process of claim 31 wherein the doped first and second semiconductor plugs are formed by introducing the dopants into the semiconductor material in situ as the semiconductor material is deposited in the first and the second windows.

33. The process of claim 32 wherein the doped first and second semiconductor plugs are formed by implanting the dopant into the semiconductor material after deposition in the first and the second windows.

34. The process of claim 31 wherein the semiconductor material comprises a crystalline semiconductor material and is selected from the group consisting of silicon, silicon-germanium, and silicon-germanium-carbon.

35. The process of claim 23 further comprising the step of forming an etch stop layer over the first layer of material, or over the second layer of material, or over both of the first and second layers.

36. The process of claim 23 further comprising the step of forming a first insulating layer above the first layer of material and forming a second insulating layer above the second layer of material.

37. The process of claim 36 wherein the first and the second insulating layers comprise etch stop layers

38. The process of claim 36 wherein the first and the second insulating layers comprise offset spacers.

39. The process of claim 23 further comprising the step of forming a diffusion barrier layer over the first device region before the at least three layers of material are formed thereover.

40. The process of claim 23 further comprising the step of forming a layer of thermal oxide on the exposed portion of the semiconductor plug and removing the layer of thermal oxide.

41. The process of claim 23 wherein the substrate is selected from the group consisting of silicon substrate and silicon on insulator substrates.

42. The process of claim 23 wherein the gate material is selected from the group consisting of doped polycrystalline silicon, doped amorphous silicon, doped polycrystalline silicon-germanium, doped amorphous silicon-germanium, doped polycrystalline silicon-germanium-carbon, doped amorphous silicon-germanium-carbon, metals, and metal-containing compounds.

43. The process of claim 42 wherein the gate material is formed on the substrate by chemical vapor deposition, electroplating, or a combination thereof.

44. The process of claim 42 wherein the metals and metal-containing compounds are selected from the group consisting of titanium, titanium nitride, tungsten, tungsten silicide, tantalum, tantalum nitride, and molybdenum.

45. A process for fabricating matched junction field-effect transistors in an integrated circuit structure comprising:

forming in a semiconductor substrate a first device region selected from the group consisting of a source region and a drain region of the junction field-effect transistors;

forming a multilayer stack comprising at least three layers of material over the first device region, wherein the second layer is interposed between the first and the third layers, and wherein the first layer is adjacent the first device region;

forming a first and a second window in the at least three layers of material, wherein said first and said second windows terminate at the first device region;

forming doped semiconductor material within the first and the second windows, thereby forming first doped and second doped semiconductor plugs in the at least three layers of material, wherein each of the first and the second semiconductor plugs has a first end and a second end, and wherein the first end of the first and the second semiconductor plugs are in contact with the first device region;

forming a second device region selected from the group consisting of a source region and a drain region at the second end of the first semiconductor plug, wherein one of the first and second device regions is a source region and the other is a drain region;

forming a third device region selected from the group consisting of a source region and a drain region at the second end of the second semiconductor plug, wherein one of the first and second device regions is a source region and the other is a drain region;

removing the second layer, thereby exposing a portion of the first and the second semiconductor plugs;

forming a doped region of opposite conductivity type surrounding the first semiconductor plug; and

forming a doped region of opposite conductivity type surrounding the second semiconductor plug.

46. An integrated circuit structure comprising:

a semiconductor substrate having a major surface formed along a plane;

a first doped region formed in the surface;

a second and a third doped region over said first doped region and of a different conductivity type than said first doped region;

a fourth doped region over said second doped region and of a different conductivity type than said second doped region;

a fifth doped region over said third doped region and of a different conductivity type than said third doped region;

an oxide layer adjacent said second doped region;

a first gate over said oxide layer; and

a second gate over said third doped region, wherein said second gate is doped a different conductivity type than said third doped region.

47. The integrated circuit structure of claim 46 wherein the first doped region comprises a first source/drain region of a MOSFET, the second doped region comprises a channel region of said MOSFET, and the fourth doped region comprises a second source/drain region of said MOSFET.

48. The integrated circuit structure of claim 46 wherein the first doped region comprises a first source/drain region of a JFET, the third doped region comprises a channel region of said JFET and the fifth doped region comprises a second source/drain region of said JFET.

49. The integrated circuit structure of claim 46 wherein the second and the third doped regions are formed within a first and a second window, respectively, formed within the semiconductor substrate.

50. The integrated circuit structure of claim 46 wherein the material of the oxide layer is selected from between silicon dioxide and silicon nitride.

51. The integrated circuit structure of claim 46 wherein the material of the first and the second gate is selected from the group consisting of doped polysilicon crystalline, doped amorphous silicon, doped silicon-germanium, doped silicon-germanium-carbon metals and metal compounds.

52. The integrated circuit structure of claim 51 wherein the metals and metal compounds are selected from the group consisting of titanium, titanium nitride, tungsten, tungsten silicide, tantalum, tantalum nitride, molybdenum, aluminum and copper.

53. An integrated circuit structure comprising first and second vertical field-effect transistors,

wherein said first vertical field-effect transistor further comprises:

a semiconductor substrate having a major surface formed along a plane;

a first doped region formed in the surface;

a second doped region over said first doped region and of a different conductivity type than said first doped region;

a third doped region over said second doped region and of a different conductivity type than said second doped region;

a dielectric layer adjacent said second doped region;

a first gate over said dielectric layer;

wherein said second vertical field-effect transistor further comprises:

a fourth doped region formed in the surface;

a fifth doped region over said fourth doped region and of a different conductivity type than said fourth doped region;

a sixth doped region over said fifth doped region and of a different conductivity type than said fifth doped region; and

a second gate over said fifth doped region and of a different conductivity type than said fifth doped region.

54. The integrated circuit structure of claim 53 wherein the first doped region comprises a first source/drain region of a MOSFET, the second doped region comprises a channel region of said MOSFET, and the third doped region comprises a second source/drain region of said MOSFET.

55. The integrated circuit structure of claim 53 wherein the fourth doped region comprises a first source/drain region of a JFET, the fifth doped region comprises a channel region of said JFET, and the sixth doped region comprises a second source/drain region of said JFET.

56. The integrated circuit structure of claim 53 wherein the second and the fifth doped regions are formed within a first and a second window, respectively, formed within the semiconductor substrate.

57. The integrated circuit structure of claim 53 wherein the material of the dielectric layer is selected from among silicon dioxide and silicon nitride.

58. The integrated circuit structure of claim 53 wherein the material of the first and the second gate is selected from the group consisting of doped polysilicon crystalline, doped amorphous silicon, doped silicon-germanium, doped silicon-germanium-carbon metals, and metal compounds.

59. The integrated circuit structure of claim 58 wherein the metals and metal compounds are selected from the group consisting of titanium, titanium nitride, tungsten, tungsten silicide, tantalum, tantalum nitride, molybdenum, aluminum and copper.

60. An integrated circuit structure comprising first and second vertical field-effect transistors,

wherein said first vertical field-effect transistor further comprises:

a semiconductor substrate having a major surface formed along a plane;

a first doped region formed in the surface;

a second doped region over said first doped region and of a different conductivity type than said first doped region;

a third doped region over said second doped region and of a different conductivity type than said second doped region;

a first gate layer proximate said second doped region;

wherein said second vertical field-effect transistor further comprises:

a fourth doped region formed in the surface;

a fifth doped region over said fourth doped region and of a different conductivity type than said fourth doped region;

a sixth doped region over said fifth doped region and of a different conductivity type than said fifth doped region; and

a second gate layer over said fifth doped region and of a different conductivity type than said fifth doped region.

wherein said first gate layer is electrically isolated from said second doped region by a dielectric layer, and wherein said second gate layer is in direct contact with said fifth doped layer.

61. The integrated circuit structure of claim 60 wherein the first doped region comprises a first source/drain region of a MOSFET, the second doped region comprises a channel region of said MOSFET, and the third doped region comprises a second source/drain region of said MOSFET.

62. The integrated circuit structure of claim 60 wherein the fourth doped region comprises a first source/drain region of a JFET, the fifth doped region comprises a channel region of said JFET, and the sixth doped region comprises a second source/drain region of said JFET.

63. The integrated circuit structure of claim 60 wherein the second doped region forms a channel of the first vertical field-effect transistor, and wherein the fifth doped region forms a channel region of the second vertical field-effect transistor.

64. A junction field-effect transistor structure comprising:

a semiconductor substrate having a major surface formed along a plane;

a first doped region formed in the surface, wherein the first doped region is of a first conductivity type;

a second doped region formed over said first doped region and of a second conductivity type;

a third doped region over said second doped region and of a first conductivity type; and

a gate region of the first conductivity type over said second doped region.

65. The junction field-effect transistor structure of claim 64 wherein the first doped region comprises a first source/drain region of a JFET, the second doped region comprises a channel region of said JFET, and the third doped region comprises a second source/drain region of said JFET.

66. An integrated circuit structure comprising:

a semiconductor substrate having a major surface formed along a plane;

a first doped region formed in the surface;

a first insulating layer over said first doped region;

a first etch stop layer over said first insulating layer;

a second insulating layer over said first etch stop layer;

a second etch stop layer over said second insulating layer;

a third insulating layer over said second etch stop layer;

a second doped region formed in a window extending from said third insulating region through said first insulating region, and wherein said second doped region is of a first conductivity type;

a third doped region over said second doped region, wherein said third doped region is of a second conductivity type;

a fourth doped region formed adjacent said second doped region, wherein said fourth doped region is of a second conductivity type.